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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,949	07/29/2003	Brian Reed	ARTCP042	1786

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,949	REED ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-15,18 and 19* is/are rejected.

7)☒ Claim(s) *1,9,10,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: in claim 1, the Applicant only recites the **results** of the operation of the circuit instead of reciting the steps of the method for protecting an input buffer. The claim should be recites: "applying a tolerance high voltage to an I/O pad etc...". Positive recitation is required.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 7, 14 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 3, the recitation "wherein p-supply is prevented from supplying current to the input buffer when an input voltage to the input buffer is tolerant HIGH" is indefinite because it is not clear what it is meant by. According to figure 5 of the present application. When the voltage at the input pad (406) is high, transistors (510) and (506) are turned off thus, there is no current flowing through the input buffer. The "p-supply" at node 412 does not prevent current from lowing though the input buffer.

Regarding claims 7, 14 and 20, the recitation "further comprising **the operation of using a generator** to design **a** the voltage tolerant input buffer" is indefinite because it is not clear how the "**a generator**" is used to design the voltage tolerant input buffer". The Applicant is requested to show where is the "a generator" in figure 5 and to explain how the generator is used to design the voltage tolerant input buffer as recited.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-6, 8, 11-13, 15, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Wert (US Pat. 6,271,703).

Regarding claims 1, 2 and 3, figure 2 of Wert shows a "method" for protecting an input buffer, comprising the operations of:

lowering a current (transistor 220d is off) from a p-supply (node 7) to an input buffer (220c, 220b) when an input voltage to the input buffer is tolerant HIGH, wherein the p-supply is a voltage supplied to a p-channel transistor (220c) in the input buffer;

setting the p-supply to a particular voltage when the input voltage to the input buffer is tolerant HIGH, the particular voltage at node being at a specific value (Vdd-2Vth) such that input transistors within the input buffer do not experience overstress voltages (col. 3, lines 45-59). The overstress voltages have values higher than an internal voltage of a Ring I/0 wherein the input buffer is located. Because transistors (220c) and (220d) are turned off, there is no current flowing through the input buffer.

Regarding claim 4, the p-supply (at node 7) is controlled using a p- supply p-channel transistor (220d).

Regarding claim 5, figure 2 of Wert shows that the p-supply p-channel transistor (220d) is turned OFF when the input to the input buffer is tolerant HIGH, and wherein the p-supply p-channel transistor turns ON when the input to the input buffer is LOW.

Regarding claim 6,when the input voltage is low, transistor (220d) is turned on, the voltage at node (7) is set to (Vdd) and when the input voltage is high, the voltage at node (7) is set to Vdd minus a threshold voltage value.

Regarding claims 8, 11, 12 and 13, figure 2 of Wert shows voltage tolerant circuit for protecting an input buffer, comprising:

an n-channel pass gate transistor (220a) having a first terminal coupled to a pad (200), a second terminal coupled an input of an input buffer (220b, 220c), and a gate coupled to an internal "ring voltage (Ring Vdd)" (Vdd); and

a p-supply p-channel transistor (220d) having a gate coupled to the pad , a first terminal coupled to Ring Vdd, and a second terminal coupled to a p-supply of the input buffer (7), wherein the p-supply is a voltage supplied to a p-channel transistor in the input buffer. The input buffer is inverter (220b, 220c).

Regarding claims 15, 18 and 19, figure 2 of Wert shows a voltage tolerant architecture, comprising:

an input buffer (220b, 220c) having an input, an output, and a p-supply, wherein the p-supply (7) is a voltage supplied to a p-channel transistor (220c) in the input buffer; and

a voltage tolerant I/O circuit having an n-channel pass gate transistor (220a) having a first terminal coupled to a pad I/0 and a second terminal coupled an input of an input buffer, and a

p-supply p-channel transistor (220d) having a gate coupled to the pad I/0, a first terminal coupled to Ring Vdd (Vdd), and a second terminal coupled to the p-supply (7) of the input buffer. The input buffer is an inverter (220b, 220c).

Allowable Subject Matter

Claims 9, 10, 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free)

Hiep Nguyen
05-14-04

TUAN T. LAM
PRIMARY EXAMINER